

## CLAIMS

1. A transistor comprising:
  - a ferromagnetic source that is formed with a  
5 ferromagnetic body from which spin-polarized conduction  
carriers are injected;
  - a ferromagnetic drain that is formed with a  
ferromagnetic body that receives the spin-polarized  
conduction carriers injected from the ferromagnetic  
10 source;
  - a semiconductor layer that is provided between  
the ferromagnetic source and the ferromagnetic drain,  
and forms a Schottky junction having a Schottky barrier  
at each junction interface with the ferromagnetic  
15 source and the ferromagnetic drain; and
  - a gate electrode that is formed associated with  
the semiconductor layer.
2. The transistor as claimed in claim 1,  
20 wherein the magnetization direction of the  
ferromagnetic source or the ferromagnetic drain is  
inverted, so that the relative magnetization direction  
of the ferromagnetic drain is made equal ("parallel  
magnetization") to or opposite ("antiparallel  
25 magnetization") to the magnetization direction of the  
ferromagnetic source.
3. The transistor as claimed in claim 1 or 2,  
wherein the ferromagnetic source and the ferromagnetic  
30 drain are made of a ferromagnetic metal.
4. The transistor as claimed in any of claims  
1 to 3, wherein the Schottky barrier appears on the  
conduction band side when the spin-polarized conduction  
35 carriers are electrons, and the Schottky barrier  
appears on the valence band side when the spin-  
polarized conduction carriers are holes, with the spin-

polarized conduction carriers being of the same conduction type as that of the semiconductor layer (an accumulation channel type).

5           5.     The transistor as claimed in any of claims  
1 to 3, wherein the Schottky barrier appears on the  
valence band side when the spin-polarized conduction  
carriers are electrons, and the Schottky barrier  
10     appears on the conduction band side when the spin-  
polarized conduction carriers are holes, with the spin-  
polarized conduction carriers being of a different  
conduction type from that of the semiconductor layer  
(an inversion channel type), the semiconductor layer  
not having an inversion layer formed therein.

15           6.     The transistor as claimed in claim 4,  
wherein, with a voltage not being applied between the  
gate electrode and the ferromagnetic source, the  
Schottky barrier restrains the spin-polarized  
20     conduction carriers from being injected to the  
semiconductor layer due to tunneling and heat radiation,  
the transistor being of the accumulation channel type.

            7.     The transistor as claimed in claim 4 or 6,  
25     wherein a voltage is applied to the gate electrode, so  
that the spin-polarized conduction carriers of the  
ferromagnetic source are injected to the semiconductor  
layer by tunneling the Schottky barrier at the  
interface between the ferromagnetic source and the  
30     semiconductor layer, the transistor being of the  
accumulation channel type.

            8.     The transistor as claimed in claim 4,  
wherein, with a voltage not being applied to the gate  
35     electrode, the Schottky barrier restrains the spin-  
polarized conduction carriers from being injected to  
the semiconductor layer due to heat radiation, while

the spin-polarized conduction carriers of the ferromagnetic source are injected to the semiconductor layer by tunneling the Schottky barrier, the transistor being of the accumulation channel type.

5

9. The transistor as claimed in claim 4 or 8, wherein, with a voltage being applied to the gate electrode, the spin-polarized conduction carriers of the ferromagnetic source tunnels the Schottky barrier at the interface between the ferromagnetic source and the semiconductor layer, so as to control a current that is generated between the ferromagnetic source and the ferromagnetic drain, the transistor being of the accumulation channel type.

15

10. The transistor as claimed in claim 5, wherein, with a voltage not being applied between the gate electrode and the ferromagnetic source, the Schottky barrier restrains the spin-polarized conduction carriers from being injected to the semiconductor layer due to tunneling and heat radiation, the transistor being of the inversion channel type.

11. The transistor as claimed in claim 5 or 10, wherein a voltage is applied to the gate electrode to form an inversion layer in the semiconductor layer, so that the spin-polarized conduction carriers of the ferromagnetic source are injected to the semiconductor layer due to at least one of heat radiation and tunneling, the transistor being of the inversion channel type.

12. The transistor as claimed in claim 5, wherein, even with a voltage not being applied to the gate electrode, an inversion layer is formed in the semiconductor layer, and the spin-polarized conduction carriers of the ferromagnetic source are injected to

the semiconductor layer due to at least one of heat radiation and tunneling, the transistor being of the inversion channel type.

5           13.    The transistor as claimed in claim 5 or 12,  
              wherein, with a voltage being applied to the gate  
              electrode, the spin-polarized conduction carriers of  
              the ferromagnetic source are injected from the  
10           ferromagnetic source to the semiconductor layer due to  
              at least one of heat radiation and tunneling, so as to  
              control a current generated between the ferromagnetic  
              source and the ferromagnetic drain, the transistor  
              being of the inversion channel type.

15           14.    The transistor as claimed in any of claims  
              4 to 13, wherein the spin-polarized conduction carriers  
              injected to the semiconductor layer are spin-polarized  
              in accordance with the spin polarization rate at the  
              Fermi energy of the ferromagnetic source, the  
20           transistor being of the accumulation channel type or  
              the inversion channel type.

              15.    The transistor as claimed in any of claims  
              4 to 14, wherein:  
25           when the relative magnetization state between the  
              ferromagnetic source and the ferromagnetic drain is  
              parallel magnetization, an electric resistance due to  
              spin-dependent scattering of the spin-polarized  
              conduction carriers injected from the ferromagnetic  
30           source is low in the ferromagnetic drain;  
              when the relative magnetization state between the  
              ferromagnetic source and the ferromagnetic drain is  
              antiparallel magnetization, the electric resistance due  
              to spin-dependent scattering of the spin-polarized  
35           conduction carriers injected from the ferromagnetic  
              source is high in the ferromagnetic drain,  
              the transistor being of the accumulation channel

type or the inversion channel type.

16. The transistor as claimed in any of claims 1 to 15, wherein trans-conductance can be controlled in accordance with the relative magnetization direction of the ferromagnetic drain with respect to the ferromagnetic source, with the same bias being applied.

17. The transistor as claimed in any of claims 4 to 16, wherein, when the ferromagnetic source and the ferromagnetic drain exhibit parallel magnetization, the transistor has a threshold voltage that is defined as a gate voltage for generating a predetermined current between the ferromagnetic source and the ferromagnetic drain, with a voltage being applied to the gate electrode,

the transistor being of the accumulation channel type or the inversion channel type.

18. A transistor comprising:

a ferromagnetic source that is made of a half metal exhibiting a metallic band structure for one of the spins ("metallic spin band") while exhibiting a semiconductor-like or insulator-like band structure for the other spin ("semiconductor spin band"), the half metal being a ferromagnetic body, spin-polarized conduction carriers being injected from the ferromagnetic source;

a ferromagnetic drain that is made of a half metal and receives the spin-polarized conduction carriers injected from the ferromagnetic source;

a semiconductor layer that is provided between the ferromagnetic source and the ferromagnetic drain, and is joined to the ferromagnetic source and the ferromagnetic drain; and

a gate electrode that is formed associated with the semiconductor layer.

19. The transistor as claimed in claim 18,  
wherein the ferromagnetic source and the ferromagnetic  
drain form a Schottky junction having a Schottky  
5 barrier at the interface between the semiconductor  
layer and the metallic spin band in the half metal.

20. The transistor as claimed in claim 18 or 19,  
wherein:

10 with the conduction carriers having the same  
conduction type as the conduction type of the  
semiconductor layer ("accumulation channel type"),  
when the conduction carriers are electrons, the  
Schottky barrier formed by the metallic spin band  
15 appears on the conduction band side; and  
when the conduction carriers are holes, the  
Schottky barrier formed by the metallic spin band  
appears on the valence band side.

20 21. The transistor as claimed in claim 18 or 19,  
wherein:

with the conductive carriers having a different  
conduction type from the conduction type of the  
semiconductor layer ("inversion channel type"), the  
25 semiconductor layer not having an inversion layer  
formed therein,  
when the conduction carriers are electrons, the  
Schottky barrier appears on the valence band side; and  
when the conduction carriers are holes, the  
30 Schottky barrier appears on the conduction band side.

22. The transistor as claimed in claim 18 or 19,  
wherein, at the junction between the semiconductor  
layer and the ferromagnetic source and drain, the  
35 semiconductor spin band of the half metal has a wider  
band gap than the band gap of the semiconductor layer.

23. The transistor as claimed in claim 18 or 19,  
wherein:

at the junction between the semiconductor layer  
and the ferromagnetic source and drain,

5 the semiconductor spin band of the half metal  
forms an energy barrier against the semiconductor  
layer;

when the conduction carriers are electrons, the  
energy barrier appears at least on the conduction side;  
10 and

when the conduction carriers are holes, the  
energy barrier appears at least on the valence band  
side.

15 24. The transistor as claimed in any of claims  
18 to 23, further comprising

a contact (a "non-magnetic contact") that is made  
of a non-magnetic metal or a non-magnetic conductor  
formed associated with the ferromagnetic source and the  
20 ferromagnetic drain.

25. The transistor as claimed in claim 24,  
wherein:

the non-magnetic contact forms a junction between  
25 metals or an ohmic junction associated with the  
metallic spin band; and

the non-magnetic contact forms a junction  
structure between a semiconductor and a metal serving  
as an energy barrier, or between a metal and an  
30 insulator, associated with the semiconductor spin band.

26. The transistor as claimed in claim 20,  
wherein, with a voltage not being applied between the  
gate electrode and the ferromagnetic source, the  
35 Schottky barrier formed by the metallic spin band  
restrains the conduction carriers in the metallic spin  
band from being injected to the semiconductor layer due

to tunneling and heat radiation,  
the transistor being of the accumulation channel  
type.

5           27. The transistor as claimed in claim 20 or 26,  
wherein, with a voltage being applied to the gate  
electrode, the conduction carriers in the metallic spin  
band of the ferromagnetic source tunnel the Schottky  
barrier formed at the interface between the  
10 ferromagnetic source and the semiconductor layer, and  
are injected to the semiconductor layer,  
the transistor being of the accumulation channel  
type.

15           28. The transistor as claimed in claim 20,  
wherein:  
with a voltage not being applied to the gate  
electrode,  
the Schottky barrier restrains the conduction  
20 carriers in the metallic spin band from being injected  
to the semiconductor layer due to heat radiation; and  
the conduction carriers in the metallic spin band  
of the ferromagnetic source tunnel the Schottky barrier  
and are then injected to the semiconductor layer,  
25 the transistor being of the accumulation channel  
type.

29. The transistor as claimed in claim 20 or 28,  
wherein  
30 with a voltage being applied to the gate  
electrode,  
the conduction carriers in the metallic spin band  
of the ferromagnetic source tunnel the Schottky barrier  
formed at the interface between the ferromagnetic  
35 source and the semiconductor layer, so as to control a  
current that is generated between the ferromagnetic  
source and the ferromagnetic drain,

the transistor being of the accumulation channel type.

30. The transistor as claimed in claim 20,  
5 wherein the energy barrier formed by the semiconductor spin band due to the non-magnetic contact restrains conduction carriers that have spins parallel to the semiconductor spin band of the ferromagnetic source from being injected to the semiconductor layer due to  
10 tunneling and heat radiation, the conduction carriers being injected from the non-magnetic contact formed along the ferromagnetic source,

the transistor being of the accumulation channel type.

15

31. The transistor as claimed in claim 21,  
wherein, with a voltage not being applied between the gate electrode and the ferromagnetic source, the Schottky barrier restrains the conduction carriers in  
20 the metallic spin band from being injected to the semiconductor layer due to tunneling and heat radiation,

the transistor being of the inversion channel type.

25 32. The transistor as claimed in claim 21 or 31, wherein, with a voltage being applied to the gate voltage so as to form an inversion layer in the semiconductor layer, the conduction carriers in the metallic spin band of the ferromagnetic source are  
30 injected from the ferromagnetic source to the semiconductor layer due to at least one of heat radiation and tunneling,

the transistor being of the inversion channel type.

35

33. The transistor as claimed in claim 21, wherein:

with a voltage not being applied to the gate electrode,

the semiconductor layer has an inversion layer formed therein; and

5 the conduction carriers in the metallic spin band of the ferromagnetic source are injected to the semiconductor layer due to at least one of heat radiation and tunneling,

10 the transistor being of the inversion channel type.

34. The transistor as claimed in claim 21 or 33, wherein, with a voltage being applied to the gate electrode, the conduction carriers in the metallic spin  
15 band of the ferromagnetic source are injected from the ferromagnetic source to the semiconductor layer due to at least one of heat radiation and tunneling,

the transistor being of the inversion channel type.

20

35. The transistor as claimed in claim 21, wherein the energy barrier formed by the semiconductor spin band due to the non-magnetic contact restrains conduction carriers that have spins parallel to the  
25 semiconductor spin band of the ferromagnetic source from being injected to the semiconductor layer due to tunneling and heat radiation, the conduction carriers being injected from the non-magnetic contact formed along the ferromagnetic source,

30 the transistor being of the inversion channel type.

36. The transistor as claimed in claim 20 or 21, wherein the spin polarization rate of conduction  
35 carriers that is determined by the ratio of the number of conduction carriers having one of the spins injected from the metallic spin band of the ferromagnetic source

to the semiconductor layer to the number of conduction carriers having the other one of the spins injected from the non-magnetic contact, formed as opposed to the ferromagnetic source, to the semiconductor layer via  
5 the semiconductor spin band of the ferromagnetic source, can be controlled by adjusting the energy gap of the semiconductor spin band of the ferromagnetic source or the height of a barrier formed with the semiconductor spin band of the ferromagnetic source or the film  
10 thickness of the ferromagnetic source, the barrier height being seen from the non-magnetic contact,  
the transistor being of the accumulation channel type or the inversion channel type.

15 37. The transistor as claimed in any of claims 20 to 36, wherein:

when the relative magnetization state between the ferromagnetic source and the ferromagnetic drain is parallel magnetization, the metallic spin band of the  
20 ferromagnetic drain can conduct the conduction carriers injected from the metallic spin band of the ferromagnetic source to the semiconductor layer; and

when the relative magnetization state between the ferromagnetic source and the ferromagnetic drain is  
25 antiparallel magnetization, the energy barrier formed by the semiconductor spin band of the ferromagnetic drain restrains the conduction carriers, injected from the metallic spin band of the ferromagnetic source to the semiconductor layer, from conduction,

30 the transistor being of the accumulation channel type or the inversion channel type.

38. The transistor as claimed in any of claims 20 to 37, wherein, when the ferromagnetic source and  
35 the ferromagnetic drain exhibit parallel magnetization, the transistor has a threshold voltage that is defined as a gate voltage for generating a predetermined

current between the ferromagnetic source and the ferromagnetic drain, with a voltage being applied to the gate electrode,

the transistor being of the accumulation channel  
5 type or the inversion channel type.

39. The transistor as claimed in any of claims 18 to 38, wherein trans-conductance can be controlled in accordance with the relative magnetization direction  
10 of the ferromagnetic drain with respect to the ferromagnetic source, with the same bias being applied.

40. The transistor as claimed in any of claims 1 to 39, wherein the ferromagnetic source and the  
15 ferromagnetic drain are formed through growth or deposition on the semiconductor layer.

41. The transistor as claimed in any of claims 1 to 39, wherein the ferromagnetic source and the  
20 ferromagnetic drain are by introducing magnetic elements into the semiconductor layer.

42. A memory device comprising  
the transistor as claimed in any of claims 1 to  
25 41,

using the transistor, information being stored in accordance with the relative magnetization direction of the ferromagnetic drain with respect to the ferromagnetic source,

30 the information stored in the transistor being detected based on the trans-conductance of the transistor depending on the relative magnetization direction of the ferromagnetic drain with respect to the ferromagnetic source.

35

43. A memory device comprising:  
the transistor as claimed in any of claims 1 to

41;

a first line that is connected to the gate electrode;

a second line that is connected to the  
5 ferromagnetic drain; and

a third line that grounds the ferromagnetic source.

44. A memory device comprising:  
10 the transistor as claimed in any of claims 1 to 41;

a first line that is connected to the gate electrode;

a second line that is connected to the  
15 ferromagnetic drain;

a third line that grounds the ferromagnetic source;

an output terminal that is formed at one end of the second line; and

20 a fourth line that branches from the second line and is connected to a power source via a load.

45. The memory device as claimed in claim 43 or 44, further comprising

25 a first extra line and a second extra line that cross each other on the transistor or in the vicinity of the transistor, being electrically insulated.

46. The memory device as claimed in claim 43 or  
30 44, wherein the first extra line and the second extra line, or one of the first extra line and the second extra line is replaced with the first line and the second line, or one of the first line and the second line.

35

47. The memory device as claimed in claim 45 or 46, wherein the magnetization of the ferromagnetic

source or the ferromagnetic drain is inverted by a magnetic field that is induced by applying a current to the first extra line and the second extra line, or the first line and the second line that replace the first  
5 extra line and the second extra line, or one of the first line and the second line that replaces one of the first extra line and the second extra line and the other one of the first extra line and the second extra line that is not replaced, so that the relative  
10 magnetization state between the ferromagnetic source and the ferromagnetic drain is changed to rewrite information.

48. The memory device as claimed in any of  
15 claims 43 to 47, wherein:

when the ferromagnetic source and the ferromagnetic drain exhibit parallel magnetization, a voltage that is higher than the threshold voltage is applied to the first line; and  
20 information is read out, based on the size of a drain current at the transistor when a predetermined bias is applied between the ferromagnetic source and the ferromagnetic drain.

49. The memory device as claimed in any of  
25 claims 44 to 47, wherein information is read out with an output voltage that is obtained based on a voltage drop due to the load caused by a drain current generated at the transistor when a voltage higher than  
30 the threshold voltage is applied to the gate electrode via the first line, the ferromagnetic source and the ferromagnetic drain exhibiting parallel magnetization.

50. A memory circuit comprising:  
35 the transistors as claimed in any of claims 1 to 41, the transistors being arranged in a matrix fashion;  
first lines that ground the respective

ferromagnetic sources;

a plurality of word lines that connect the respective gate electrodes of the transistors that are arranged in the column direction; and

5 a plurality of bit lines that connect the respective ferromagnetic drains of the transistors that are arranged in the row direction.

51. A memory circuit comprising:

10 the transistors as claimed in any of claims 1 to 41, the transistors being arranged in a matrix fashion; first lines that ground the respective ferromagnetic sources;

15 a plurality of word lines that connect the respective gate electrodes of the transistors that are arranged in the column direction;

a plurality of bit lines that connect the respective ferromagnetic drains of the transistors that are arranged in the row direction;

20 output terminals each formed at one end of each of the bit lines; and

second lines that branch from the respective bit lines and are connected to a power source via a load.

25 52. The memory circuit as claimed in claim 50 or 51, further comprising

30 a first extra line and a second extra line that crosses each other on each of the transistors or in the vicinity of each of the transistors, the first extra line and the second extra line being electrically insulated.

53. The memory circuit as claimed in claim 52, wherein the first extra line and the second extra line, or one of the first extra line and the second extra line is replaced with the corresponding word line and the corresponding bit line, or one of the corresponding

word line and the corresponding bit line.

54. The memory circuit as claimed in any of claims 50 to 53, wherein the magnetization of the ferromagnetic source or the ferromagnetic drain is inverted by a magnetic field that is induced by applying a current to the first extra line and the second extra line, or the word line and the bit line that replace the first extra line and the second extra line, or one of the word line and the bit line that replaces one of the first extra line and the second extra line and the other one of the first extra line and the second extra line that is not replaced, so that the relative magnetization state between the ferromagnetic source and the ferromagnetic drain is changed to rewrite information.

55. The memory circuit as claimed in any of claims 50 to 54, wherein:  
when the ferromagnetic source and the ferromagnetic drain exhibit parallel magnetization, a voltage that is higher than the threshold voltage is applied to the word line; and  
information is read out, based on the size of a drain current at the transistor when a predetermined bias is applied between the ferromagnetic source and the ferromagnetic drain.

56. The memory circuit as claimed in any of claims 51 to 54, wherein information is read out with an output voltage that is obtained based on a voltage drop due to the load caused by a drain current generated at the transistor when a voltage higher than the threshold voltage is applied to the gate electrode via the word line, the ferromagnetic source and the ferromagnetic drain exhibiting parallel magnetization.

57. The memory device or the memory circuit as claimed in any of claims 43 to 55, wherein information is rewritten by inverting the magnetization of the ferromagnetic source or the ferromagnetic drain.

5

58. A memory device comprising:

first and second transistors that are as claimed in any of claims 1 to 41;

10 a first line that collectively connects the gate electrode of the first transistor and the gate electrode of the second transistor;

a second line that is connected to a first ferromagnetic drain of the first transistor;

15 a third line that is connected to a second ferromagnetic drain of the second transistor; and

a fourth line that grounds the ferromagnetic source that is shared between the first and second transistors.

20

59. A memory circuit comprising

memory cells that are formed with the memory devices as claimed in claim 58, the memory cells being arranged in a matrix fashion.

25

60. The transistor as claimed in any of claims 1 to 3, wherein the semiconductor layer is an undoped semiconductor or an intrinsic semiconductor.

30 61. The transistor as claimed in claim 18 or 19, wherein the semiconductor layer is an undoped semiconductor or an intrinsic semiconductor.

35 62. The transistor as claimed in any of claims 4, 6 to 9, 14 to 17, 20, 22 to 30, and 36 to 41, wherein the semiconductor layer is an undoped semiconductor or an intrinsic semiconductor, the transistor being of the accumulation channel type.

63. The transistor as claimed in any of claims 5, 10 to 15, 17, 21, 31 to 41, wherein the semiconductor layer is an undoped semiconductor or an intrinsic semiconductor, the transistor being of the inversion channel type.

64. The transistor as claimed in any of claims 1 to 39, 60, and 61, wherein a channel length that is defined as the length in the carrier conducting direction in the semiconductor layer or the distance between the ferromagnetic source and the ferromagnetic drain is so short that the semiconductor layer can conduct carriers in a ballistic manner, or the channel length is equal to or shorter than the mean free path associated with carrier energy relaxation.

65. The transistor as claimed in any of claims 1 to 17, 60, and 64, further comprising a metal layer that forms a Schottky junction between the semiconductor layer and the metal layer, or a semiconductor layer that forms a Schottky junction between the ferromagnetic metal and the semiconductor layer, or a metal/semiconductor Schottky junction layer, the metal layer, the semiconductor layer, or the metal/semiconductor Schottky layer being formed at the interface between the ferromagnetic metal and the semiconductor layer.

66. The transistor as claimed in any of claims 18 to 39, 61, and 64, further comprising a metal layer that forms a Schottky junction between the semiconductor layer and the metal layer, or a semiconductor layer that forms a Schottky junction between the half metal and the semiconductor layer, or a metal/semiconductor Schottky junction layer, the metal layer, the semiconductor layer, or the

metal/semiconductor Schottky layer being formed at the interface between the half metal and the semiconductor layer.

5           67.    The transistor as claimed in any of claims  
60 to 66, wherein, when the relative magnetization of  
the ferromagnetic drain with respect to the  
ferromagnetic source is antiparallel magnetization, the  
drain current is lower than the drain current in a case  
10 of parallel magnetization.

          68.    The transistor as claimed in any of claims  
60 to 67, wherein trans-conductance can be controlled  
in accordance with the relative magnetization direction\_  
15 of the ferromagnetic drain with respect to the  
ferromagnetic source.

          69.    A memory device comprising  
the transistor as claimed in any of claims 60 to  
20 68,  
          using the transistor, information being stored in  
accordance with the relative magnetization direction of  
the ferromagnetic drain with respect to the  
ferromagnetic source,  
25           the information stored in the transistor being  
detected based on the trans-conductance of the  
transistor depending on the relative magnetization  
direction of the ferromagnetic drain with respect to  
the ferromagnetic source.

30           70.    The memory device as claimed in any of  
claims 42 to 49 and 58, wherein the transistor is as  
claimed in any of claims 60 to 68.

35           71.    The memory circuit as claimed in any of  
claims 50 to 57 and 59, wherein the transistor is as  
claimed in any of claims 60 to 68.

72. A transistor comprising:  
a source and a drain that are of a first  
conduction type, and are formed with ferromagnetic  
5 semiconductors;  
a semiconductor layer that is provided associated  
with the source and the drain, and has a channel of the  
first conduction type formed therein; and  
a gate electrode that is formed as opposed to the  
10 semiconductor layer.

73. The transistor as claimed in claim 72,  
wherein the semiconductor layer is formed with an  
undoped semiconductor or an intrinsic semiconductor.  
15

74. The transistor as claimed in claim 72 or 73,  
wherein a channel length that is defined as the length  
in the carrier conducting direction in the  
semiconductor layer or the distance between the  
20 ferromagnetic source and the ferromagnetic drain is so  
short that the semiconductor layer can conduct carriers  
in a ballistic manner, or the channel length is equal  
to or shorter than the mean free path associated with  
carrier energy relaxation.  
25

75. A transistor comprising:  
a source that is formed with a first pn junction  
between a first ferromagnetic semiconductor and a  
semiconductor layer that are of different conductive  
30 types from each other;  
a drain that is formed with a second pn junction  
between a second ferromagnetic semiconductor and the  
semiconductor layer that are of different conductive  
types from each other; and  
35 a gate electrode that is formed associated with  
the semiconductor layer.

76. The transistor as claimed in claim 75,  
wherein a channel length that is defined as the length  
in the carrier conducting direction in the  
semiconductor layer or the distance between the  
5 ferromagnetic source and the ferromagnetic drain is of  
such length that the semiconductor layer can conduct  
carriers in a ballistic manner, or the channel length  
is equal to or shorter than the mean free path for  
carrier energy relaxation.

10

77. The transistor as claimed in any of claims  
72 to 76, wherein, when the relative magnetization of  
the ferromagnetic drain with respect to the  
ferromagnetic source is antiparallel magnetization, the  
15 drain current is lower than the drain current in a case  
of parallel magnetization.

78. The transistor as claimed in any of claims  
72 to 77, wherein trans-conductance can be controlled  
20 in accordance with the relative magnetization direction  
of the ferromagnetic drain with respect to the  
ferromagnetic source.

79. A memory device comprising  
25 the transistor as claimed in any of claims 72 to  
78,

using the transistor, information being stored in  
accordance with the relative magnetization direction of  
the ferromagnetic drain with respect to the  
30 ferromagnetic source,

the information stored in the transistor being  
detected based on the trans-conductance of the  
transistor depending on the relative magnetization  
direction of the ferromagnetic drain with respect to  
35 the ferromagnetic source.

80. The memory device as claimed in any of

claims 42 to 49 and 58, wherein the transistor is as claimed in any of claims 72 to 78.

81. The memory circuit as claimed in any of  
5 claims 50 to 57 and 59, wherein the transistor is as claimed in any of claims 72 to 78.

82. A transistor comprising:  
a ferromagnetic source that is formed with a  
10 ferromagnetic body from which spin-polarized conduction carriers;  
a ferromagnetic drain that is formed with a ferromagnetic body and receives the spin-polarized conduction carriers injected from the ferromagnetic  
15 source;  
a semiconductor layer that is provided between the ferromagnetic source and the ferromagnetic drain, and form junctions with the ferromagnetic source and the ferromagnetic drain; and  
20 a gate electrode that is formed associated with the semiconductor layer.

83. The transistor as claimed in any of claims 1 to 41, 60 to 68, 72 to 78, and 82, wherein a gate  
25 insulating film formed between the gate electrode and the semiconductor layer is an insulator that is formed through oxidization or deposition.

84. The transistor as claimed in claim 83,  
30 wherein the gate insulating film contains a high dielectric constant material.

85. The transistor as claimed in claim 1 to 41, 60 to 68, 72 to 78, 82, and 84, wherein the transistor  
35 is a MISFET.

86. The transistor as claimed in any of claims

1 to 3, 8, 9, 12, 13, 18, 19, 28, 29, 33, 34, 72 to 78, and 82 to 85, wherein an impurity is added to the semiconductor layer, so that the transistor functions as a depletion-mode transistor. .